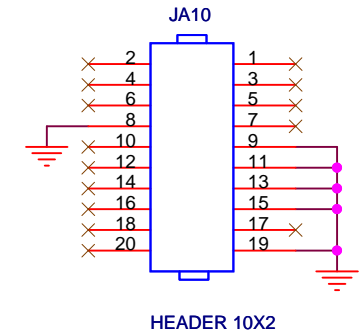
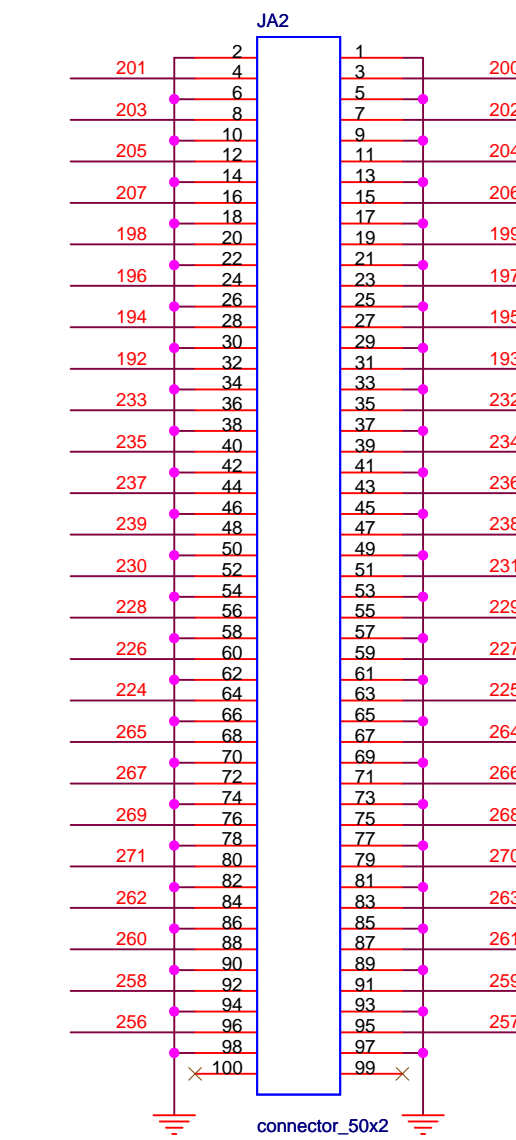
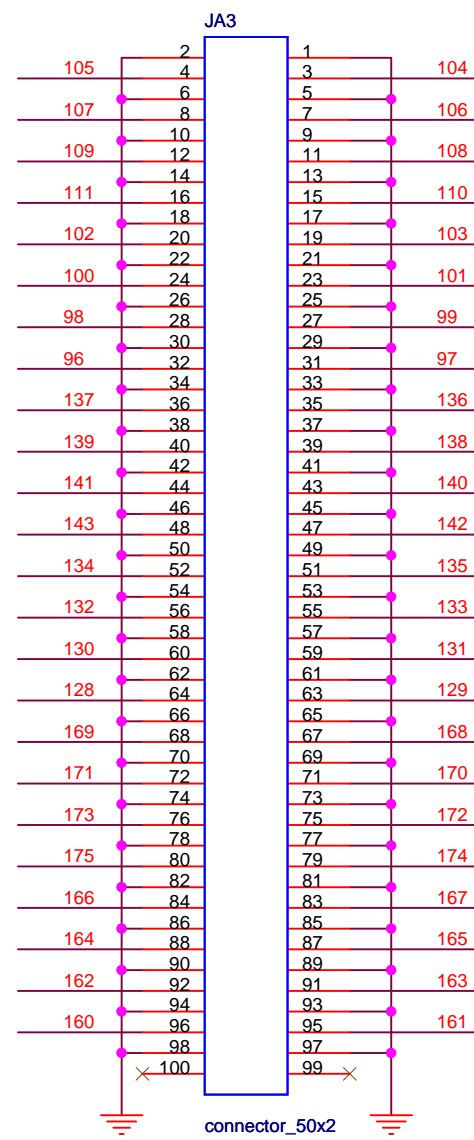
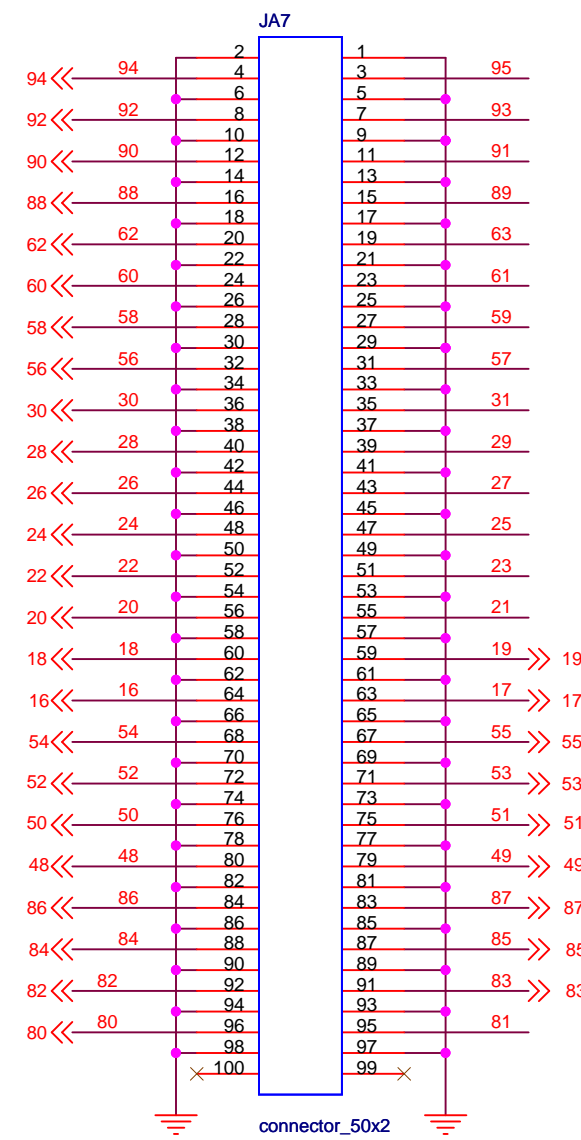
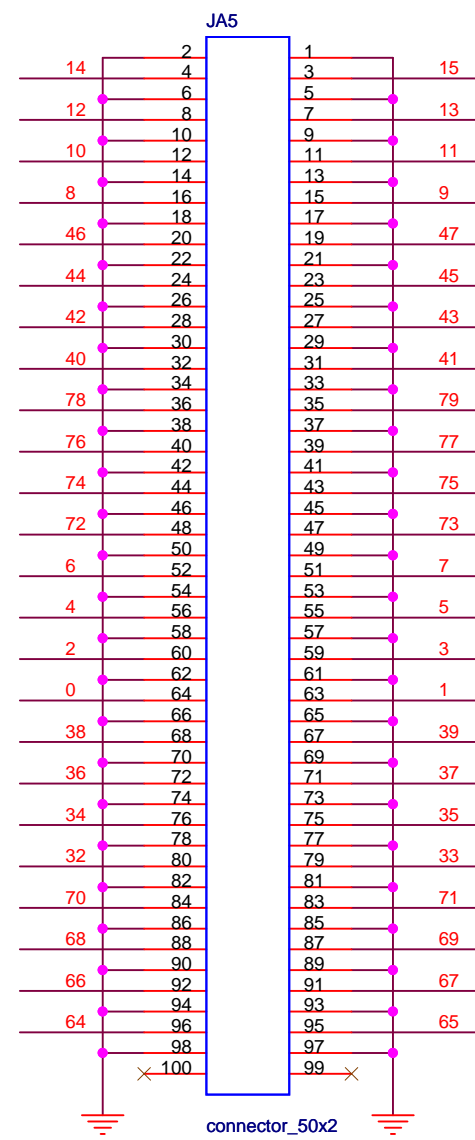
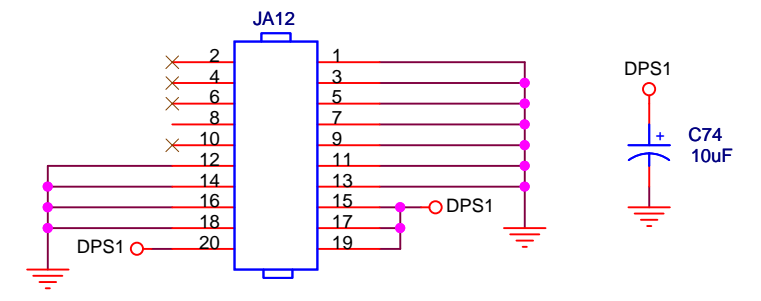


- NOTES:
1. J3 Hard Copy Header is always routed to the J4 Raceway Header. The distance between J3 and J4 (Raceway) designed to be as short as possible, about .7". For standalone testing plug the Raceway Cable into the J4 Header.
 2. J11 Header routed to the Tester FPGA only.
 3. J2 Header is routed only to the DUT Card Tester Channel connectors JA7 and JA6.
 4. A 2 x 40 pin connector (Molex - 15-45-1340 or Equiv.) will be used as a jumper. Thus installing the Molex between the J11 FPGA Tester Header and the J3 Hardcopy ASIC Header connects them. And the J2 DUT card Tester Channel will be disconnected.
 5. When the 2 x 40 Molex is installed between J2 DUT Card header and J3 Hardcopy ASIC header it connects them. Tester FPGA circuit will be disconnected.

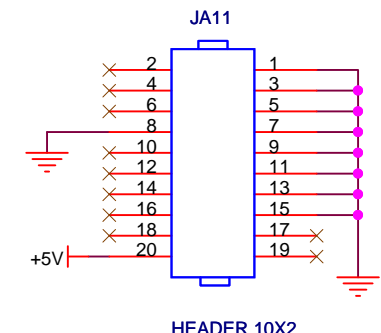
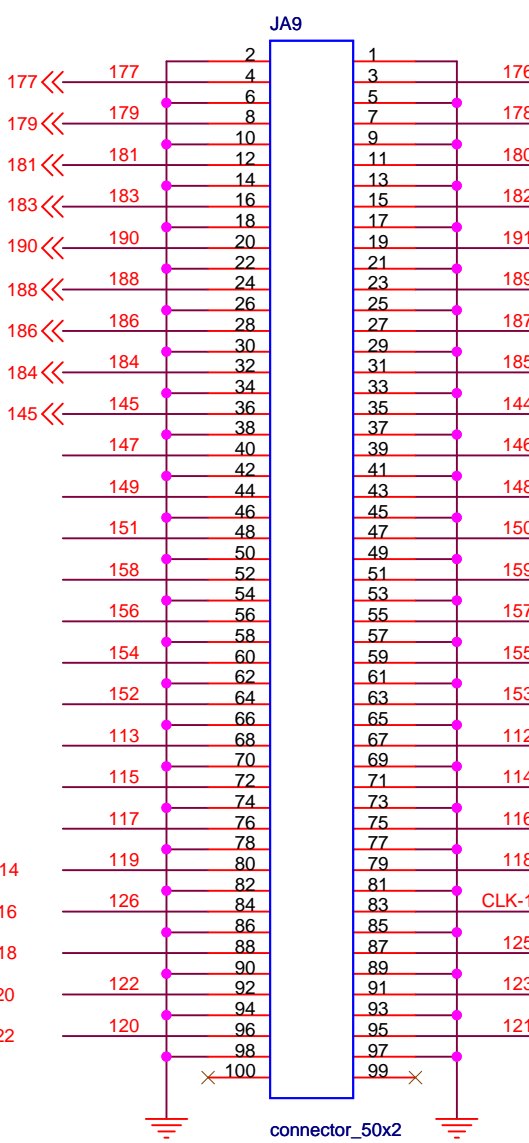
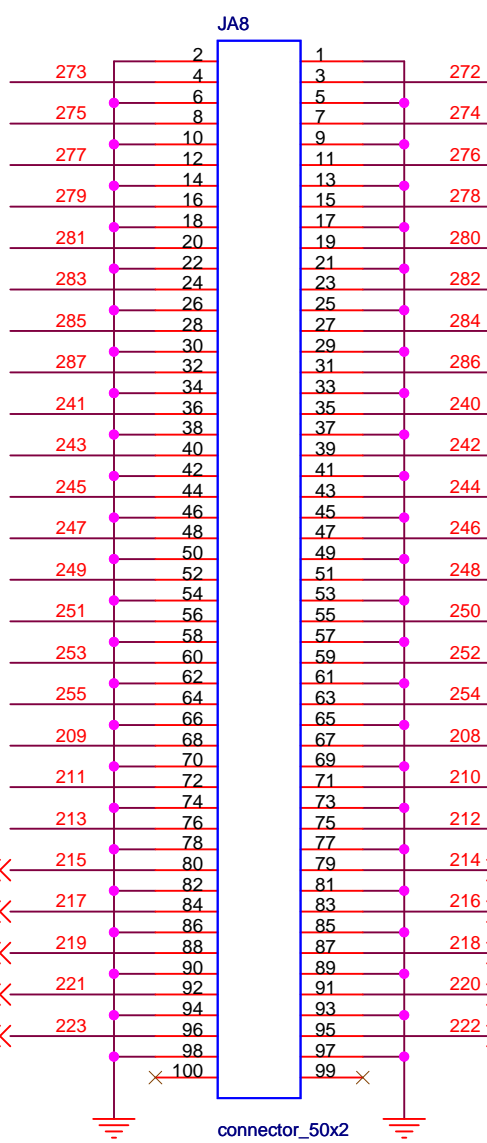
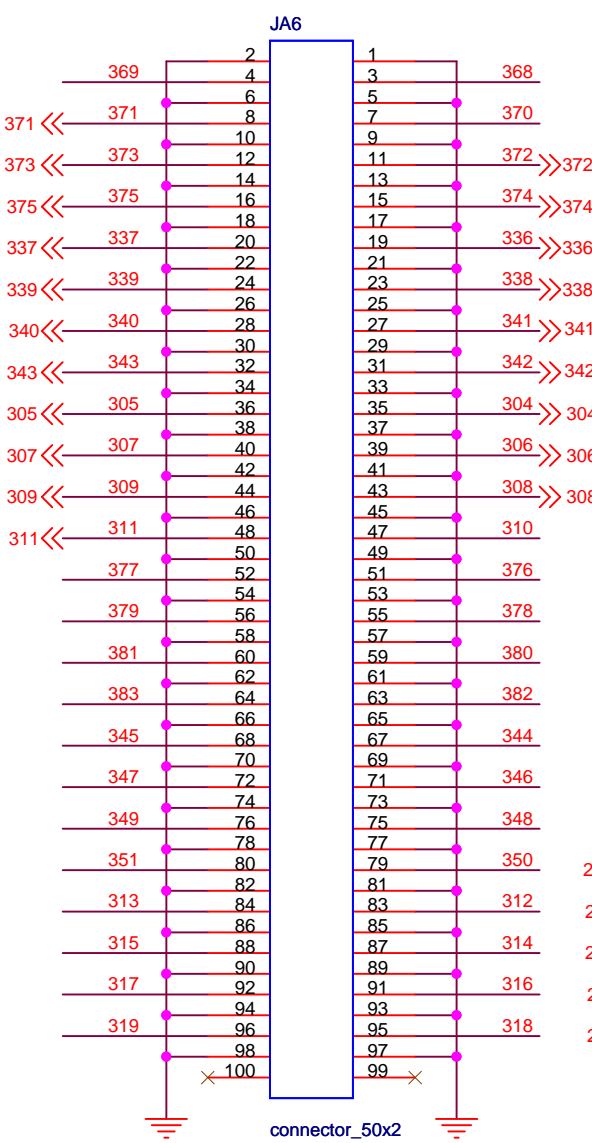
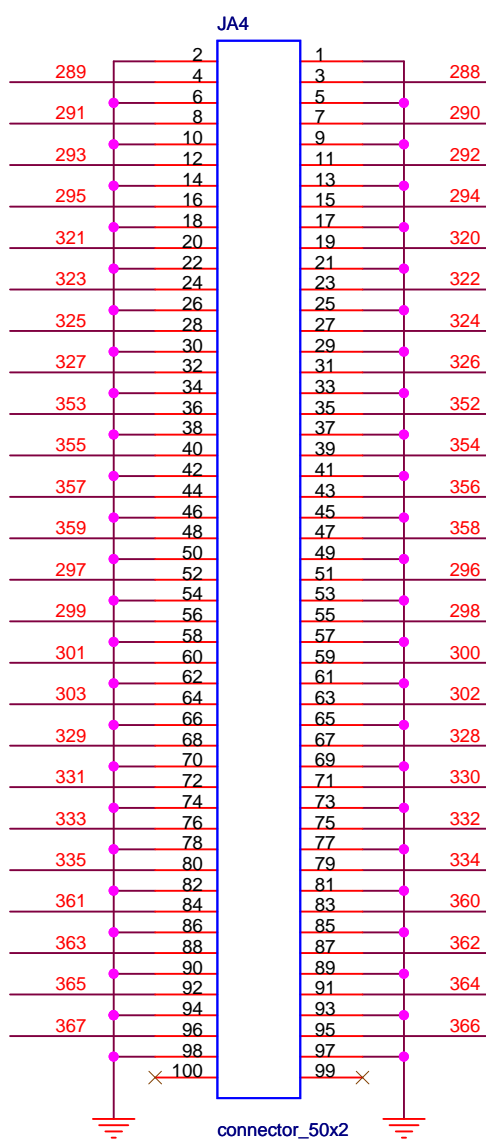
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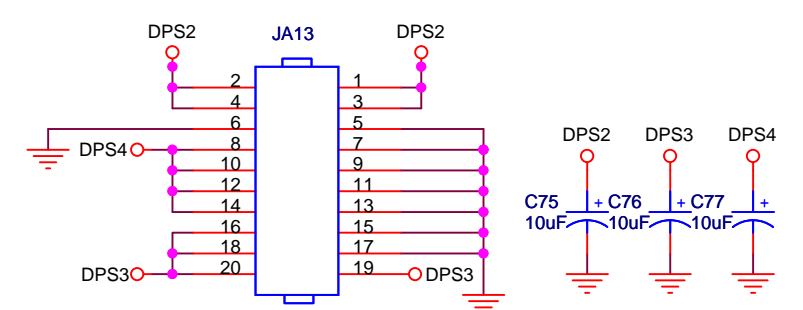
HEADER 10X2



HEADER 10X2



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