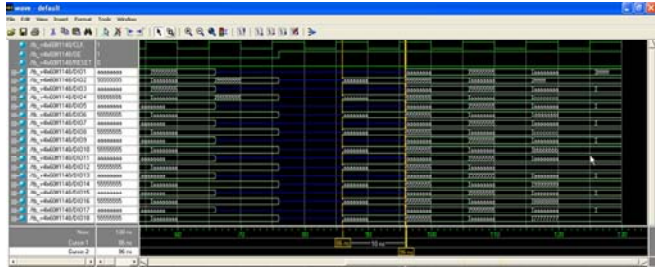


Vector Change Dump
Waveform Simulation
.vcd

test_bench_for_test_circuit_design.v

test_circuit_design.v

Mentor Graphics ModelSim
VHDL Simulator/Waveform viewer

Synopsis FPGA Express V.3.6.0
Xilinx Edition Synthesizer
Windows 98 SE only

.edf – EDIF file

Xilinx Development Software ISE V. 4.2
PMR (place map route) and program

.bit
.rbt (ASCII)

Xilinx iMPACT
Configurator

.svf Serial Vector Format
JTAG programming file
FPGA industry standard
IEEE1149

.bit
.rbt (ASCII)
.svf (JTAG IEEE1149)

.bsm (Boundary Scan)

LMO IC Tester
Built in JTAG IEEE1149 Programmer

4

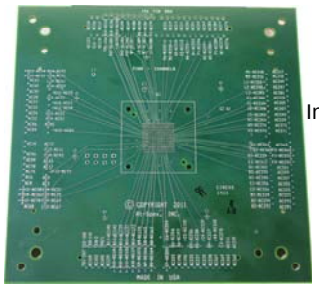
TDI, TDO, TMS, TCK

JTAG Pins

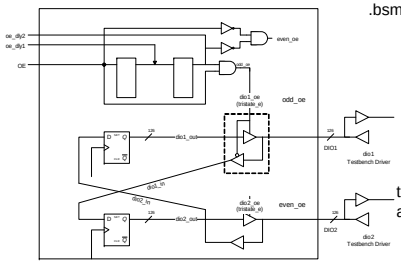
XILINX®

XCS20 TQ144 Spartan

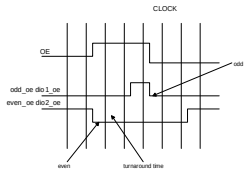
Pin 1



DUT Tester
Interface Card

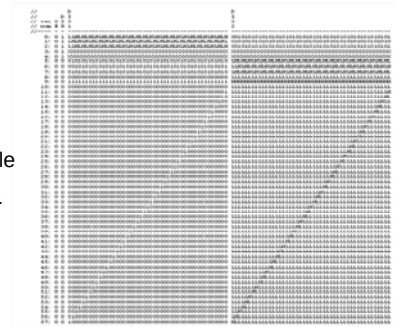


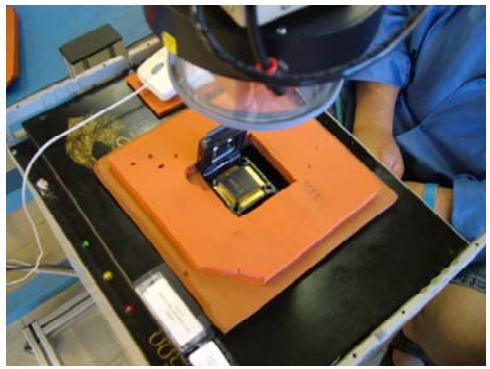
In the XCS20_TQ144
each I/O pin is
programmed with this
tester circuit, ea mimicking
an actual tester Pin Driver/
Comparator




JEDEC Vector
Post Processor
C++/Verilog

.cvf configurable
vector format





**Thermostream Temperature Forcing System above test head**
**Yamaichi Clam-shell**
**Test socket shown open**

**Programmable soak time**
**+/- 1 degree accuracy**

**Single DUT Insertion for -45 to +85C Industrial or -55 to +125 Military Temperature Range at min/max Test Limits over guaranteed Data Sheet Test Conditions**

**Protective foam forms a seal**

**Spartan Family Recommended Operating Conditions**

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage relative to GND, $T_J$ = 0°C to +85°C | Commercial | 4.75 | 5.25 | V |
| | Supply voltage relative to GND, $T_J$ = –40°C to +100°C(1) | Industrial | 4.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage(2) | TTL inputs | 2.0 | $V_{CC}$ | V |
| | | CMOS inputs | 70% | 100% | $V_{CC}$ |
| $V_{IL}$ | Low-level input voltage(2) | TTL inputs | 0 | 0.8 | V |
| | | CMOS inputs | 0 | 20% | $V_{CC}$ |

**Spartan Family DC Characteristics Over Operating Conditions**

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage @ $I_{OH}$ = –4.0 mA, $V_{CC}$ min | TTL outputs | 2.4 | - | V |
| | High-level output voltage @ $I_{OH}$ = –1.0 mA, $V_{CC}$ min | CMOS outputs | $V_{CC}$ – 0.5 | - | V |
| $V_{OL}$ | Low-level output voltage @ $I_{OL}$ = 12.0 mA, $V_{CC}$ min(1) | TTL outputs | - | 0.4 | V |
| | | CMOS outputs | - | 0.4 | V |
| $V_{DR}$ | Data retention supply voltage (below which configuration data may be lost) | | 3.0 | - | V |
| $I_{CCO}$ | Quiescent FPGA supply current(2) | Commercial | - | 3.0 | mA |
| | | Industrial | - | 6.0 | mA |
| $I_L$ | Input or output leakage current | | –10 | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested) | | - | 10 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V (sample tested) | | 0.02 | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 5V (sample tested) | | 0.02 | - | mA |

LMO IC Tester
384 I/O AC/DC Parametrics and Functional Test
19ps resolution,
+/-100 ps edge placement accuracy
12 bit DC PMU calibrated ¼ lsb