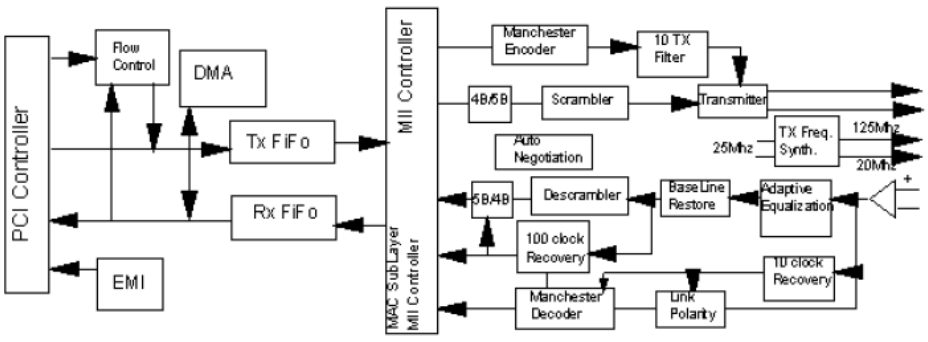
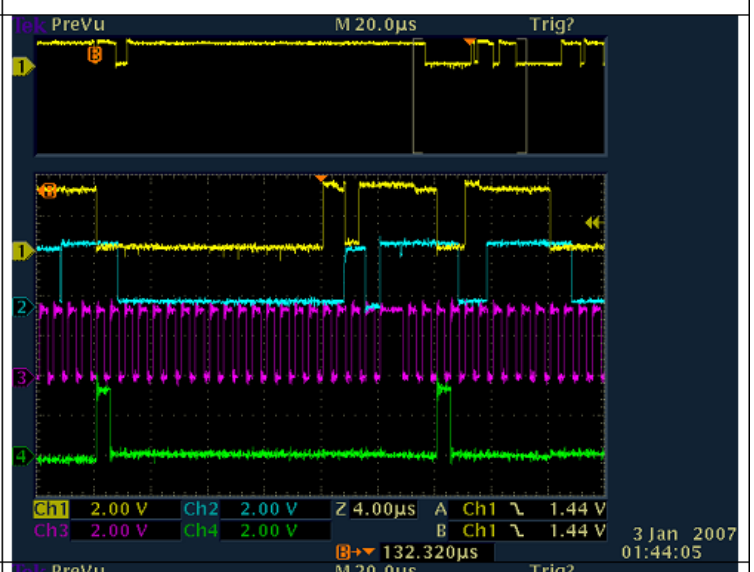
```
PCICLK RSTn FRAMEn IRDYn GNTn AD[31:0] CBEB[3:0] TRDYn IDSEL DEVSELn REQn STOPn PERRn SERRn PAR INTAn PMEn BRA[16:0] BRD[4:0] BrCSn BrOEn BrWEn LEDLK LEDC1 LEDSpd Vccdct Vauxdct BD6 BD7 EECS;
//                                                                                D                                                      LLLVV
//          P   F                                                        CCCC       E                                                      EEECA
//          C   R I                                                      ////  T I  V     S P   S     I       B       BB           B  BBB      DDDCU
//          I R A R G     A         A         A        A                 BBBB  R D  S R   T E   E     N P     R       RR           R  RRR      MMMDX   E
//          C S M D N     D         D         D        D                 EEEE  D S  E E   O R   R P   T M     A       AA           D  COW      111ED BBE
//          L T E Y T     3         2         1        0                 nnnn  Y E  L Q   P R   R A   A E     1       00           0  SEE      LFSTE DDC
//          K n n n n     1         3         5        7                 3210  n L  n n   n n   n R   n n     6       87           4  nnn      KDPET 67S
//          - - - - -   --------   --------  -------- --------          ----  - -  - -   - -   - -   - -    ----------------- -----  ---      ----- ---
            ;ldlc.100
//Wait 100 clocks for a PCI REQ# from UUT after TX turned on
Wait_TX_Desc_REQ:
            K 1 X X 1   XXXXXXXX   XXXXXXXX  XXXXXXXX XXXXXXXX        XXXX  1 0  1 L   X X   X X   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...
            ;Match.Wait_TX_Desc_REQ
            K 1 X X 1   XXXXXXXX   XXXXXXXX  XXXXXXXX XXXXXXXX        XXXX  1 0  1 X   X X   X X   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...
            ;JmpFail.No_TX_Desc_REQ
//GNT# REQ#
            K 1 X X 0   XXXXXXXX   XXXXXXXX  XXXXXXXX XXXXXXXX        XXXX  1 0  1 X   X X   X X   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...
//          ;ldlc.17
//Wait 16 clocks for an access after bus granted to UUT PCI System Architecture p. 61
Wait_Memory_Access_1:
            K 1 L H 0   LHLLLLLL   LLLLLLLL  LLLLLLLL LLLLLLLL        LHHL  1 0  1 X   X X   X X   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...
           ;Match.Wait_Memory_Access_1
//Delays driving bus one clock--klunk vs. PCI timing
            K 1 X X 0   XXXXXXXX   XXXXXXXX  XXXXXXXX XXXXXXXX        XXXX  1 0  1 X   X X   X X   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...
            ;JmpFail.No_TX_Desc_Access
//Read TXDES0--own bit set for STE10
            K 1 L L 0   10000000   00000000  00000000 00000000        XXXX  0 0  0 X   X X   X 1   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  .... ...      .....  ...
//Read TXDES1, 2, 3
//was 32 byte size = 6 bytes x 2 addr + 2 bytes length + 18 data bytes; CSR18 default is 64bytes
            K 1 L L 0   01100010   00000000  00000000 01000000        LLLL  0 0  0 X   X X   X 1   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...
//Buffer Address
            K 1 L L 0   10100000   00000000  00000000 00000000        LLLL  0 0  0 X   X X   X 0   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    ................  ..... ...     .....  ...
            K 1 H L 0   00000000   00000000  00000000 00000000        LLLL  0 0  0 X   X X   X 0   X X    XXXXXXXXXXXXXXXXX  XXXXX XXX      XXX10 XXX
@@          . . u u .   ........   ........  ........ ........        ....  u .  u u   u u   u .   u u    .................  ..... ...      ..... ...

//---------------------------------------------------------------
```

Table 3: Test Vector Micro-Instructions, UUT Syncronization. Here is the test vector code to do a TX Descriptor Read

1 Wait for STE to issue a PCI request as the Initiator (STE asserts REQn Output Low on vector label Wait_TX_Desc_REQ:).
2 The tester which is now the Target, then gives the STE its GNTn.
3 Wait up to 16 PCI Clocks on vector labled Wait_Memory_Access_1 to Match the actual DUT response with its expected response, which is,
that the STE issues the transmit descriptor base address 0x40000000 on the PCI AD bus,
and the Memory Read command (0x6) on the command bus, and asserts FRAME#
4 Insert dummy turn-around per the Read Transaction waveform
5 Then the Target gives the STE Bus Master its DEVSELn and TRDYn by driving them to logic 0, the STE will then begin
reading the TX Descriptor first of 4 D-Words TDES0 (pointed to by the transmit descriptor address) on the next PCI Klunk.
Note reading means the tester has to drive the TXDES0 own bit MSB 31 Hi.
TRDYn is used to hold off the master until the target is ready. On the next the PCI Clock, the tester provides TXDES1 = 0x62000040
(page 40 of 66)which sets the buffer size. 40= 0100 0000 sets the 2 byte count to 2**6= 64 bytes. 64 bytes/4 bytes per
D-word= Burst Length of 16. On the next PCI Clock TXDES2, which is the TX Buffer Address 0xA0000000, is written into (read by) the STE

Figure 3: PCI Ethernet Controller with Integrated PHY



Picture #	Trace Description	Trace
1 Shows CBEB0 indicative of a 16 word write, followed by a read of CSR5 and then STE writes two more FCS words to RX buffer.	Trace 1: FRAME# Trace 2: TRDY# Trace 3: PCI CLK Trace 4: C/BEB0#	
2 This view shows the two word write of the latter part of the scope picture above. The STE reads the TX Buffer again and then does a write to TX DES0.	Trace 1: FRAME# Trace 2: TRDY# Trace 3: PCI CLK Trace 4: C/BEB#