



Figure 91: 400 MHz Programmable Clock

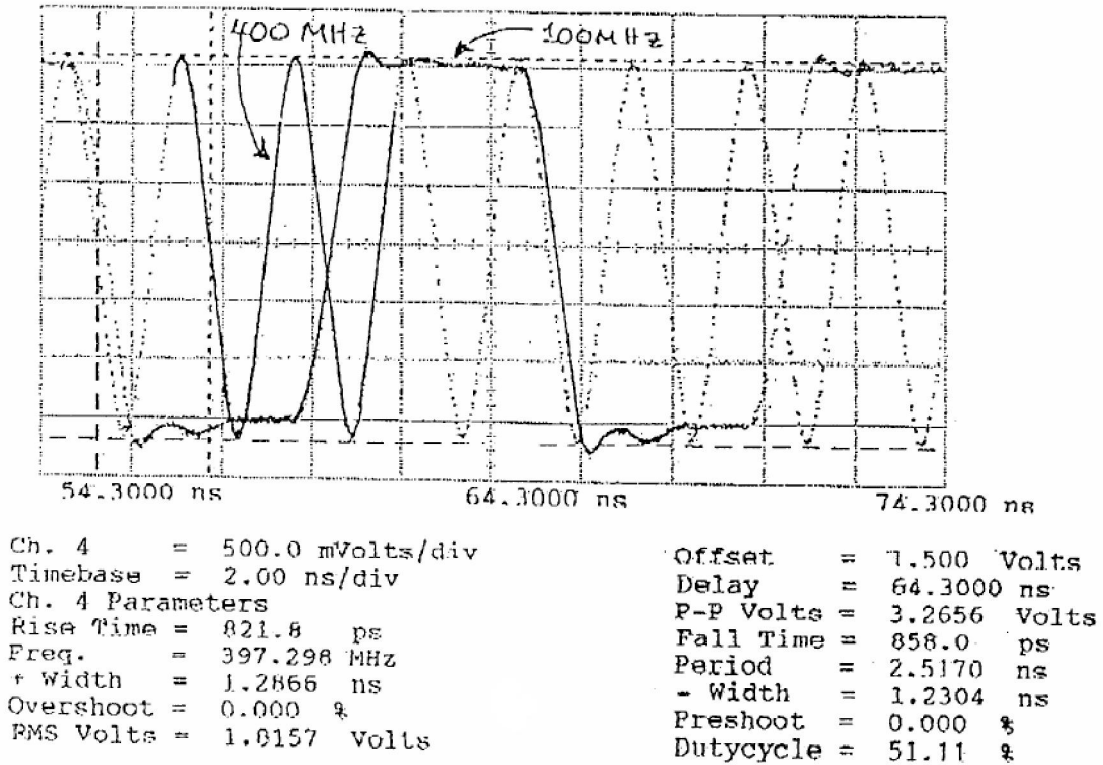


Figure 92: 2ns Minimum Pulse Width

